Notice of Allowability	Application No.	Applicant(s)	
	10/826,725	LAI ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an amendment filed on 04/12/2006*.

2. ☒ The allowed claim(s) is/are *5-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *09/801,350* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

The following is an examiner's statement of reasons for indicating allowance of claims 5 and 6: The prior art teaches an electrostatic discharge protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising a silicon controlled rectifier circuit which comprises a first connection terminal, a second connection terminal, and a third connection terminal; and an anti-latch-up circuit comprising a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, whereby when a to-be-protected IC is powered by the voltage source, an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit; wherein the SCR circuit comprises a P-type substrate, an N well formed in the p-type substrate; a first P+ doped region; a first N+ doped region formed in the P-type substrate; a second N+ doped region; a second P+ doped region; and a third N+ doped region; wherein the anti-latch-up circuit comprises a PMOS transistor, a resistor and a capacitor. However, the prior does not teach that the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when the to-be-protected IC is powered by the voltage source. This feature in combination with the rest of the claim limitation is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 8: The prior art teaches an electrostatic discharge protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising a silicon controlled rectifier circuit which comprises a first connection terminal, a second connection terminal, and a

third connection terminal; and an anti-latch-up circuit comprising a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, whereby when a to-be-protected IC is powered by the voltage source, an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit; wherein the SCR circuit comprises a P-type substrate, an N well formed in the p-type substrate; a first P+ doped region; a first N+ doped region formed in the P-type substrate; a second P+ doped region; a third P+ doped region; and a second N+ doped region. However, the prior art does not disclose that the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when to-be-protected IC is powered by the voltage source. This feature in combination with the rest of the claim limitation is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 11: The prior art teaches an electrostatic discharge protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising a silicon controlled rectifier circuit which comprises a first connection terminal, a second connection terminal, and a third connection terminal; and an anti-latch-up circuit comprising a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, whereby when a to-be-protected IC is powered by the voltage source, an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit; wherein the SCR circuit comprises a P-

type substrate, an N well formed in the p-type substrate; a first P+ doped region; a first N+ doped region formed in the P-type substrate; a second P+ doped region; a third P+ doped region, wherein an additional PMOS transistor with a source/drain region and a gate electrode of the p-type LVTSCR circuit is formed between the second P+ doped region and the third P+ doped region; and a second N+ doped region. However, the prior art does not disclose that the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when to-be-protected IC is powered by the voltage source. This feature in combination with the rest of the claim limitation is not anticipated or rendered obvious by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
04/28/2006

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